Cascadable Gain Block AG41

DESCRIPTION

Sanland's AG41 is a high performance InGaP HBT MMIC amplifier utilizing a Darlington configuration with an active bias network. The active bias network provides stable current over temperature and process Beta variations. Designed to run directly from a 5V supply, the AG41 does not require a dropping resistor as compared to typical Darlington amplifiers. The AG41 product is designed for high linearity 5V gain block applications that require small size and minimal external components. It is internally matched to 50Ω.

KEY FEATURES

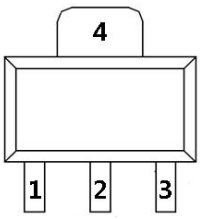
- **Wideband Flat Gain to 4GHz**
- **36 dBm Output IP3 at 1950MHz**
- **15.3 dB Gain at 1950MHz**
- **19.5 dBm P1dB at 1950MHz**
- **50 ohm Cascadeable**
- **Lead-free/Green/RoHS compliant SOT89 package**
- **Single 5V Supply**
- **ESD 1000V HBM**
- **MSL: Level 1**

RoHS Compliant & Green Package

Major Applications

- **Wireless system, IF&RF driver amplifier**

Pin Assignment



SOT89

Pin Details

Pin Number	Name	Description
1	RF IN	RF input.
2	GND	Ground.
3	RF OUT	RF output.
4	GND	Ground.

Electrical Characteristics for Application

(Vc =+5V; unless otherwise noted.)

Parameter	Specification			Units	Notes
	Min	Typ.	Max		
Gain	13.0 14.0	15.0 15.5 15.3 15.0	17.0 17.0	dB dB dB dB	240MHz 850MHz 1950MHz *2600*MHz
P-1dB	18.0	19.5 19.0		dBm dBm	1950MHz 2600MHz
OIP3	36.0 34.0	38.0 36.0 35.0		dBm dBm dBm	850MHz 1950MHz 2600MHz
Bandwidth		4000		MHz	
Input return loss		-20	-10	dB	1950MHz
Output return loss		-15	-10	dB	1950MHz
Reverse Isolation		23		dB	1950MHz
NF		4.0	5.0	dB	1950MHz
Vs		5.0	5.5	V	
Is	75	85	95	mA	
Thermal Resistance		60		℃/W	
Test Conditions：Vs=5V Is=85mA Typ. OIP3 Tone Spacing=1MHz, Pout per ton=+5 dBm TL=25℃ ZS=ZL=50 Ohms					

Absolute Maximum Ratings

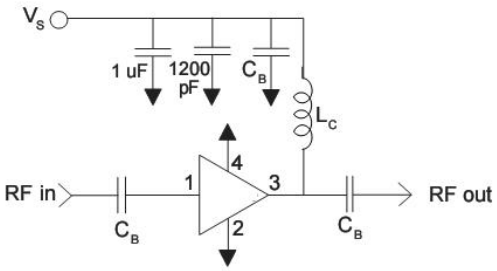
Parameter	Rating	Unit
DC Power Supply	+5.5	V
DC Supply Current at Vc	110	mA
RF Input Power	+20	dBm
Max. Operating Dissipated Power	0.66	W
Operating Ambient Temperature	-45 to +85	℃
Max. Storage Temp	+150	℃
Max. Junction Temp. (TJ)	+150	℃
Operation beyond any one of these limits may cause permanent damage.		

Important Note:

The information provided in this datasheet is deemed to be accurate and reliable only at present time. Sanland Technology Corp. reserves the right to make any changes to the specifications in this datasheet without prior notice.

Caution: ESD Sensitive
Appropriate precaution in handling, packaging
And testing devices must be observed.

Typical Performance (50 ~ 1000MHz Application Circuit)

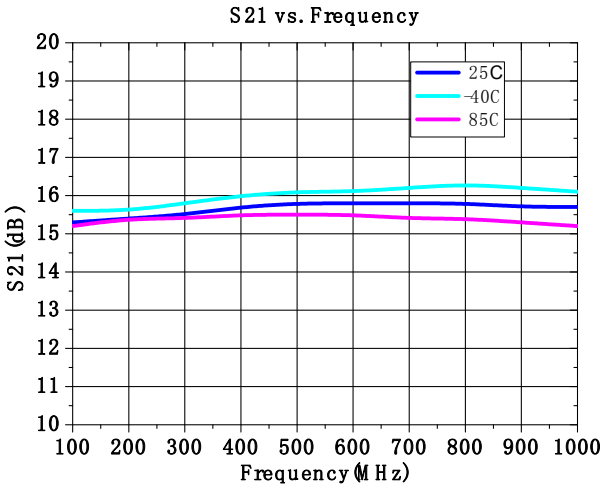


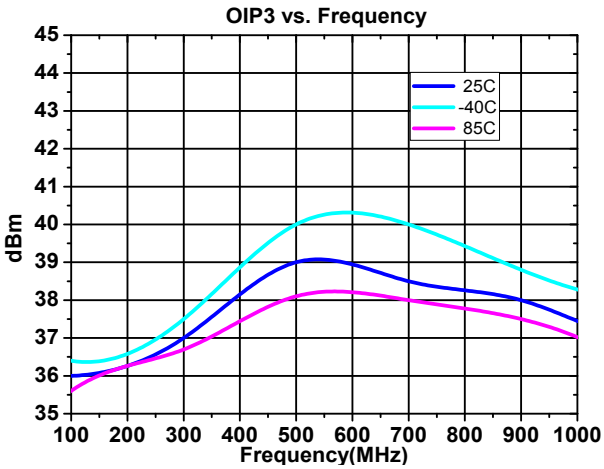
Reference Designator	BOM	Tolerance
C_B	8200 pF	±5%
L_C	1200 nH	±5%

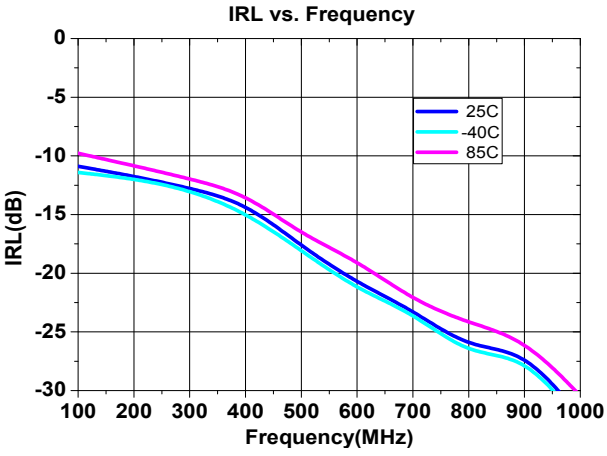
			Frequency（MHz）					
Symbol	Parameter	Unit	50	110	240	400	500	850
G	Small Signal Gain	dB	15.0	15.1	15.5	15.7	15.8	15.8
OIP_3	Output Third Order Intercept Point	dBm	36.0	36.1	36.5	38.0	39.0	38.0
P_{1dB}	Output Power at 1dB Compression	dBm	19.5	19.5	19.5	19.5	19.5	19.5
IRL	Input Return Loss	dB	-10	-12	-14	-15	-18	-25
ORL	Output Return Loss	dB	-10	-12	-12	-13	-15	-16
S_{12}	Reverse Isolation	dB	24	24	24	24	24	24
NF	Noise Figure	dB	4.2	4.2	4.1	4.0	4.0	4.1

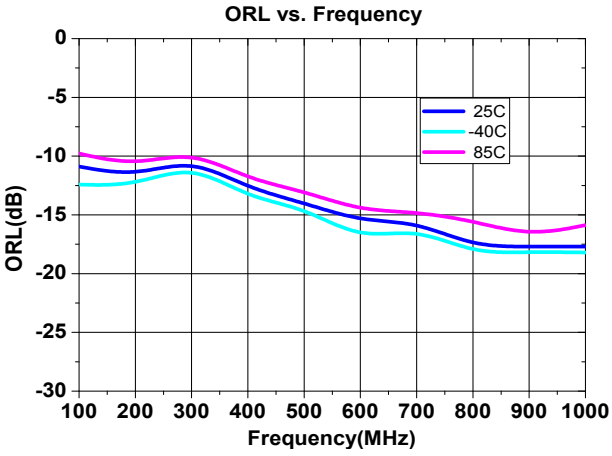
Test Conditions：Vs＝5V I_D＝80mA OIP3 Tone Spacing=1MHz, Pout per tone=5 dBm
T_L=25℃ Z_S=Z_L=50 Ohms

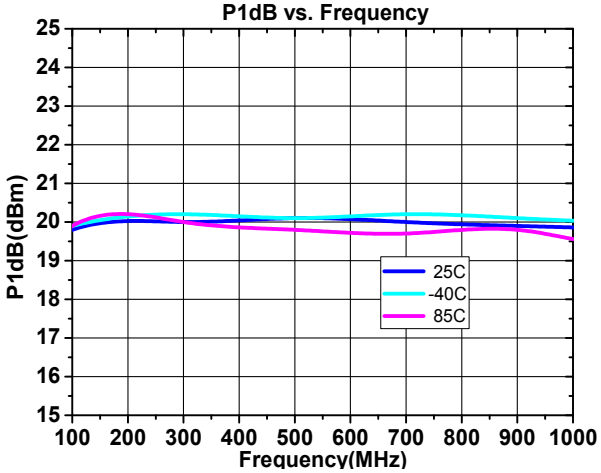
Performance Plots (50~1000MHz Application Circuit)



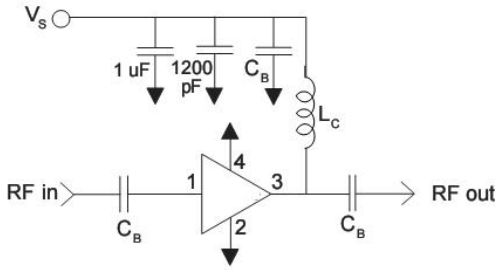








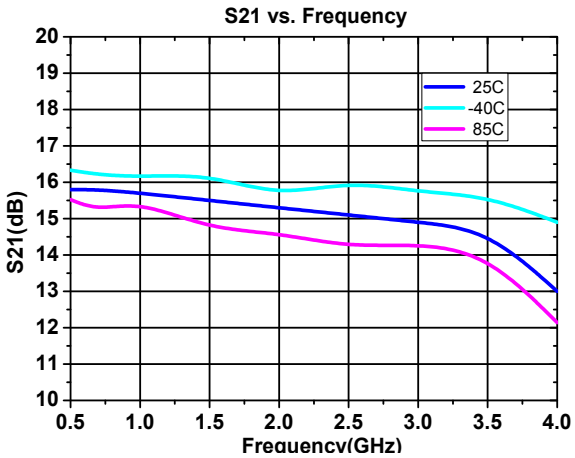
Typical Performance (0.5 ~ 3.5GHz Application Circuit)

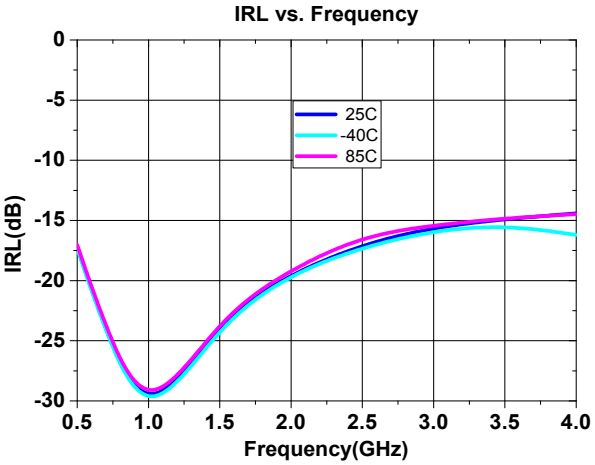


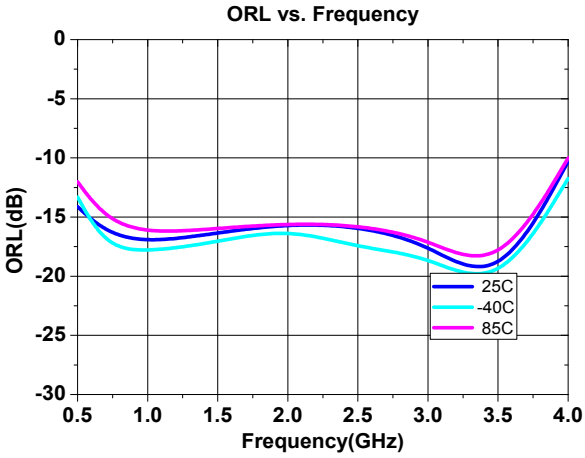
Reference Designator	BOM	Tolerance
C_B	68 pF	±5%
L_C	82 nH	±5%

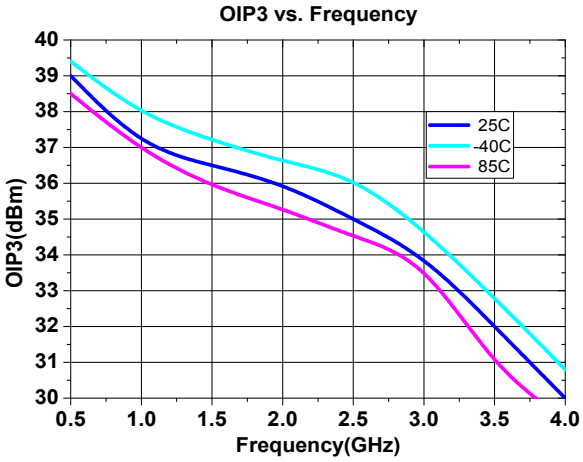
			Frequency（MHz）						
Symbol	Parameter	Unit	500	850	1950	2600	3500	4000	4800
G	Small Signal Gain	dB	15.5	15.5	15.3	15.0	14.5	14	13.7
OIP_3	Output Third Order Intercept Point	dBm	39	37	36	35	32	30	27
P_{1dB}	Output Power at 1dB Compression	dBm	19.5	19.5	19.5	19.0	18	16	12.5
IRL	Input Return Loss	dB	-17	-25	-20	-17	-16	-15	-11
ORL	Output Return Loss	dB	-15	-16	-16	-16	-18	-10	-11
S_{12}	Reverse Isolation	dB	24	23	23	23	22	22	21
NF	Noise Figure	dB	4.0	4.0	4.1	4.2	4.3	4.5	4.6
Test Conditions：Vs＝5V Is＝85mA OIP3 Tone Spacing=1MHz, Pout per tone=5 dBm T_L=25℃ Z_S=Z_L=50 Ohms									

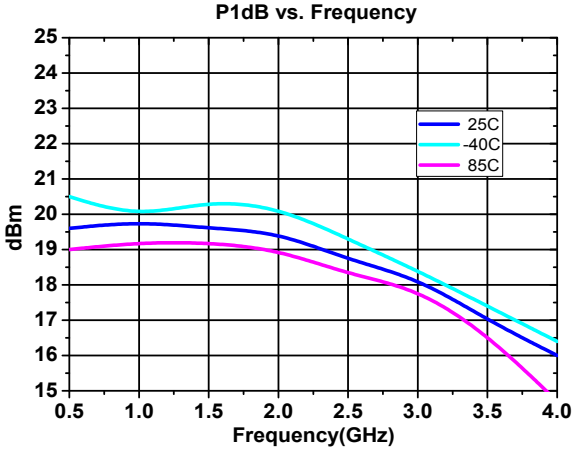
Performance Plots (0.5~3.5GHz Application Circuit)



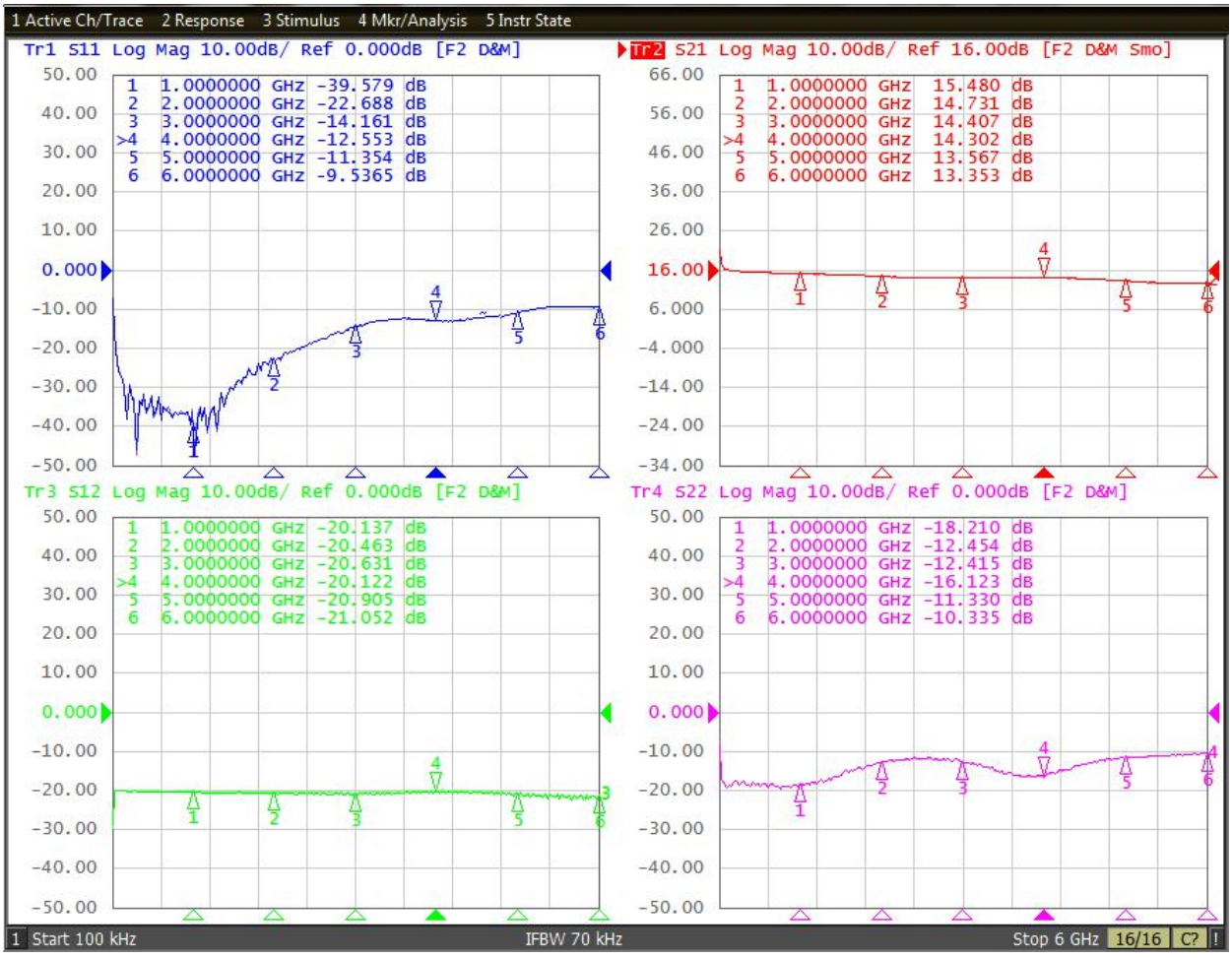




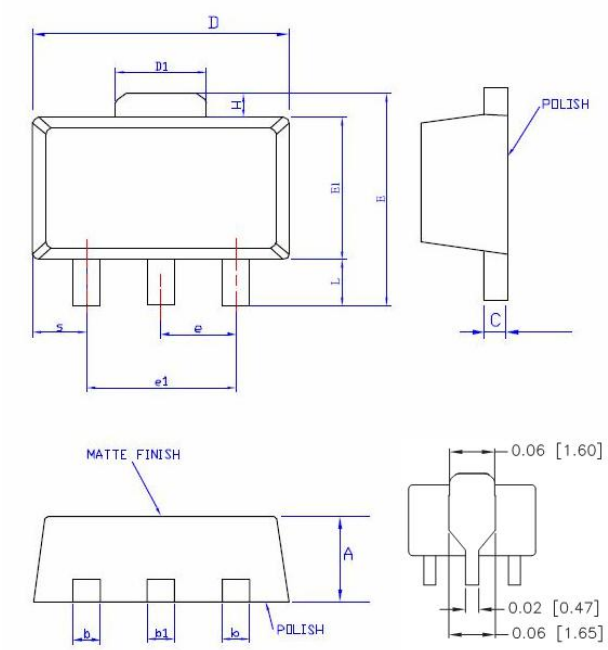




Typical Performance with Bias Tees, VS=5V, ID=85mA



Package Outline



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.40	1.50	1.60	0.055	0.059	0.063
L	0.89	1.04	1.20	0.0350	0.041	0.047
b	0.36	0.42	0.48	0.014	0.016	0.018
b1	0.41	0.47	0.53	0.016	0.018	0.020
C	0.38	0.40	0.43	0.014	0.015	0.017
D	4.40	4.50	4.60	0.173	0.177	0.181
D1	1.40	1.60	1.75	0.055	0.062	0.069
E	3.94	—	4.25	0.155	—	0.167
E1	2.40	2.50	2.60	0.094	0.098	0.102
e1	2.90	3.00	3.10	0.114	0.118	0.122
H	0.35	0.40	0.45	0.014	0.016	0.018
S	0.65	0.75	0.85	0.026	0.030	0.034
e	1.40	1.50	1.60	0.054	0.059	0.063

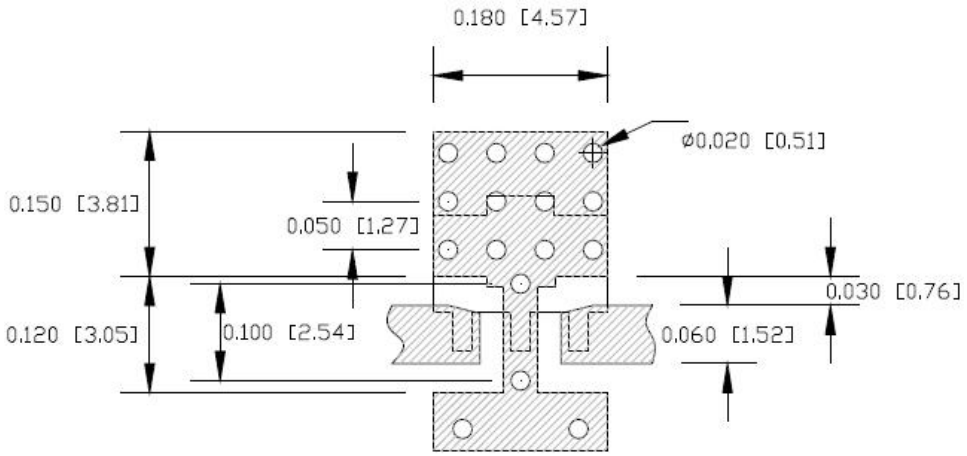
For informational purpose only and is subject to change without notice

Note：

1. Dimension and tolerance conform to ASME Y14.5M-1994.

2. Refer to JEDEC STD. MO-220 WEED-2 ISSUE B

Suggested PCB Layout



NOTES:

1. Dimensions are in inch [millimeter].
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under GND(2,4) pin for proper RF/DC grounding and thermal dissipation. Via holes could reduce lead inductance as close to ground as possible.
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.